What is claimed is:

1   Sub 1. A data transceiver node, comprising:

2   a master clock having an output at which a master clock signal is generated;

3   a timebase having an input coupled to receive said master clock signal and having

4   an output at which a downstream and upstream clock signal generated from said

5   master clock signal appears, each of upstream and downstream clock signals being

6   phase coherent with said master clock signal;

7   a downstream data input;

8   an SCDMA downstream modulator coupled to said downstream data input and

9   coupled to receive said downstream clock signal and having a chips output;

10   a downstream carrier synthesizer coupled to receive said master clock signal and

11   having a downstream carrier output at which a downstream carrier appears which is

12   phase coherent with said master clock signal;

13   a first mixer having a first input coupled to said chips output and having a second

14   input coupled to said downstream carrier output and having an output at which

15   modulated downstream signals appear for coupling to a transmission media or media

16   transmitter;

17   a second mixer having an input for coupling to a transmission medium or media

18   receiver, and having a carrier input for receiving an upstream carrier, and having

19   an output at which baseband demodulated upstream signals appear;

20   an upstream carrier synthesizer coupled to receive said master clock signal and

21   having an output at which a synthesized upstream carrier signal appears which is

22   phase coherent with said master clock signal, said output coupled to said carrier

23   input of said second mixer; and

24   an SCDMA upstream demodulator having an input coupled to said output of said

25   second mixer and having an input coupled to receive said upstream clock signal, and

26   having an output at which recovered upstream data appears, and including means for

27   correcting phase and amplitude errors in incoming constellation points transmitted

28   from other data transmission nodes located at varying distances from said data

29 transceiver, and further comprising means for achieving frame synchronization or
30 minislot boundary synchronization.

1   2. A digital data transceiver comprising:
2   a first mixer having an input for receiving code division multiplexed downstream
3   signals and having a carrier input for receiving a local downstream carrier, and
4   having a product output at which demodulated signals appear;
5   an SCDMA demodulator having an input coupled to said product output and having
6   a clock input and having a clock steering output and having a recovered downstream
7   data output;
8   a voltage controlled oscillator having an error signal input coupled to said clock
9   steering output and having a recovered clock output;
10 a clock multiplier having an input coupled to said recovered clock output and
11 having a recovered downstream clock output coupled to said clock input of said
12 SCDMA demodulator;
13 a clock divider having an input coupled to said recovered clock output and having
14 an clock output;
15 a first synthesizer having an input coupled to said clock output of said clock
16 divider and having an output coupled to said carrier input of said first mixer at
17 which a first carrier appears which is phase coherent with said recovered clock;
18 an SCDMA modulator/multiplexer having an input for receiving upstream data
19 and having a clock input coupled to said recovered clock output of said clock
20 multiplier and capable of carrying out any form of prior art ranging or other
21 process to achieve frame synchronization or alignment of minislot boundaries of said
22 data transceiver with minislot boundaries in a receiving node, and having an output
23 at which code division multiplexed upstream signals appear;
24 a second synthesizer having a clock input coupled to said clock output of said clock
25 divider and having an upstream carrier output at which an upstream carrier appears
26 which is phase coherent with said recovered clock;
27 a second mixer having an input coupled to said output of said SCDMA modulator

28 and having an input coupled to said upstream carrier output of said second

29 synthesizer, and having an output for coupling to a shared transmission media.

1   3.   A digital data transceiver comprising:

2   a master clock for generating a master downstream clock signal at a clock output

3 having a frequency which is an integer multiple of a downstream symbol or chip

4 rate, F_{ds};

5   a downstream modulator implementing any form of TDMA or CDMA multiplexing

6 or no multiplexing at all and any form of modulation, and having a clock input

7 coupled to said clock output of said master clock, and having a data input for

8 receiving downstream data and having a data output at which symbols to be

9 transmitted downstream appear;

10   a downstream mixer having a data input coupled to said data output of said

11 downstream modulator and having a carrier input for receiving a downstream

12 carrier, and having a data output for coupling to a transmission media;

13   an upstream clock generator having a clock input coupled to said clock output of

14 said master clock and having an upstream clock output at which appears an upstream

15 clock signal having a frequency which is M/N times the frequency of said downstream

16 clock signal where M and N are integers;

17   a frequency divider having a clock input coupled to said clock output of said

18 master clock and having a carrier clock output at which a carrier clock signal

19 appears;

20   a downstream carrier synthesizer coupled to receive said carrier clock signal

21 and having an output at which appears a downstream carrier signal which is phase

22 coherent with said downstream clock signal and which is coupled to said carrier

23 input of said downstream mixer;

24   an upstream carrier synthesizer having a clock input coupled to said clock output

25 of said frequency divider, and having an upstream carrier output at which appears an

26 upstream carrier signal which is phase coherent with said master downstream clock

27 signal;

28   an upstream mixer having a carrier input coupled to said upstream carrier

29   output and having an input for coupling to a transmission media, and having an output

30   at which baseband demodulated upstream signals appear;

31   an upstream demodulator/demultiplexer implementing any form of TDMA or

32   SCDMA or CDMA demultiplexing, or no demultiplexing at all if the incoming data is

33   not multiplexed, and which implements any form of demodulation, and which is

34   capable of carrying out prior art ranging or other processes to achieve frame

35   synchronization or alignment of minislot boundaries of the transmitted signal to

36   minislot boundaries in said data transceiver, and having a clock input for receiving

37   said upstream clock signal and coupled to receive said baseband demodulated

38   upstream signals, and having an output at which appears recovered upstream data.

1   4. A data transceiver, comprising:

2   a downstream mixer having an input for coupling to a transmission media and

3   having a downstream carrier input, and having an output at which baseband

4   downstream signals appear;

5   a downstream demodulator/demultiplexer which can be any conventional

6   demodulator/demultiplexer and which has an input to receive a downstream clock

7   signal and an input coupled to receive said baseband downstream signals, and an

8   output at which recovered downstream data appears and which includes conventional

9   downstream clock recovery circuitry, and a clock steering output at which appears a

10   clock steering signal;

11   a voltage controlled oscillator having a control input coupled to receive said clock

12   steering output and having a recovered downstream clock output at which a recovered

13   downstream clock signal appears;

14   an upstream clock generator having an input coupled to receive said recovered

15   downstream clock signal and having an upstream clock output at which appears an

16   upstream clock signal which is phase coherent with said downstream clock signal and

17   which has a frequency which is related to the frequency of said downstream clock

18   signal by the ratio M/N where M and N are integers;

19   a frequency divider having a clock input coupled to said upstream clock output

20   and having a carrier clock output;

21   a downstream carrier synthesizer having a clock input coupled to said carrier

22   clock output and having a downstream carrier output at which a downstream carrier

23   appears which is phase coherent with said recovered downstream clock, said

24   downstream carrier output coupled to said downstream carrier input of said

25   downstream mixer;

26   an upstream carrier synthesizer having a clock input coupled to said carrier

27   clock output, and having an upstream carrier output at which an upstream carrier

28   signal appears which is phase coherent with said recovered downstream clock;

29   an upstream mixer having an upstream carrier input coupled to said upstream

30   carrier output and having a symbol input for receiving symbols to be transmitted

31   upstream, and having an output for coupling to a transmission media; and

32   an upstream modulator/multiplexer which is capable of TDMA or SCDMA or

33   CDMA multiplexing using any prior art circuitry and is capable of carrying out

34   ranging or other prior art processes of achieving frame synchronization or

35   alignment of upstream minislot boundaries with minislot boundaries at a receiving

36   node, and having an input coupled to said upstream clock output and having an input

37   for receiving upstream data and having an output coupled to said symbol input of said

38   upstream mixer.

39

1   5. A digital data communication system comprising:

2   a shared transmission medium;

3   in a first node:

4   a master clock for generating a downstream clock signal having a

5   frequency F_{DS};

6   a first upstream clock generation means having an input coupled to

7   receive said downstream clock signal from said master clock for generating at an

8   output an upstream clock signal having a frequency F_{US} which has a frequency

9   equal to $(M/N)^*F_{DS}$ where M and N are integers;

10   first means having an input for receiving downstream data to be

11   transmitted on said shared transmission media and having an input coupled to

12   receive said downstream clock signal, and having an output coupled to said shared

13. transmission medium, for generating a downstream carrier from said

14 downstream clock signal and using said downstream clock signal to organize said

15 downstream data into a plurality of symbols, and, if necessary, using said

16 downstream clock signal to time division or code division multiplex said symbols

17 if data from more than one source must be kept separate, and modulating said

18 symbols onto said downstream carrier and launching the modulated downstream

19 signals into said shared transmission medium;

20 in one or more second nodes:

21 second means having an input coupled to said shared transmission media

22 and having clock recovery means for recovering said downstream clock signal

23 from modulated downstream signals on said shared transmission media and

24 outputting the recovered downstream clock signal at a dowstream clock output,

25 said second means functioning to use said recovered downstream clock signal to

26 demodulate said modulated downsteam signals and recover said downstream data

27 or, if necessary, to demultiplex said demodulated downstream signals to generate

28 demultiplexed signals and recover said downstream data from said demultiplexed

29 signals;

30 a second upstream clock generation means having an input coupled to

31 receive said recovered downstream clock and having an output at which said phase

32 lock loop generates an upstream clock signal having a frequency $F_{US} =$

33 $(M/N)*F_{DS}$ where M and N are integers, said upstream clock signal being

34 generated from said downstream clock signal so as to be phase coherent with said

35 downstream clock signal;

36 third means having an input for receiving upstream data bits and having

37 an input coupled to receive said upstream clock signal, said third means for using

38 said upstream clock signal to organize said upstream data bits into one or more

39 chips or symbols to be transmitted to said first node, and, if necessary, for using

40 said upstream clock signal to multiplex said chips or symbols of upstream data

41 using time division or code division multiplexing into a plurality of timeslots or

42 result vectors to be transmitted, and for generating a phase coherent upstream

43 carrier from said upstream clock signal, and for modulating said timeslots or

44   result vectors onto said upstream carrier to generate upstream signals and

45   launching said upstream signals into said shared transmission medium and

46   translating the frequency of the upstream signals to a selected frequency in the

47   upstream band and filtering the Fourier spectrum of said upstream signals to

48   limit the spectrum to a band of frequencies at a center frequency that does not

49   interfere with other signals on said shared transmission medium;

50   and said first node further comprising:

51   fourth means having an input coupled to receive said upstream clock

52   signal from said first upstream clock generation means and having an input

53   coupled to said shared transmission media and including means for generating a

54   local upstream carrier from said upstream clock generated by said first

55   upstream clock generation means which has the same frequency as said upstream

56   carrier generated in each of said second nodes, said fourth means for recovering

57   said upstream data from said demodulated upstream signals, including using said

58   upstream clock to demultiplex said upstream signals if necessary prior to

59   recovering the upstream data.

1   6. A modem for use at a headend of a system for bidirectional communication of digital

2   data over a transmission media, comprising:

3   a master clock for generating a master clock signal;

4   means for generating upstream and downstream clock signals which are phase

5   coherent with said master clock signal, said upstream clock signal having a

6   frequency which is M/N times the frequency of said downstream clock signal, where

7   M and N are integers;

8   means coupled to receive said downstream clock signal for using it to transmit

9   downstream data over said transmission media; and

10   means coupled to receive said upstream clock signal for using it to receive

11   upstream data transmitted over said transmission media.

1   7. A modem for use as a remote node in a bidirectional communication system having

2   a headend and a plurality of remote node coupled to said headend by a transmission media,

3   comprising:

4   first means for recovering a downstream clock from data transmitted by said

5   headend over said transmission media and for using said recovered downstream clock

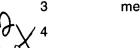6   to recover downstream data;

7   second means for using said recovered downstream clock to generate an upstream

8   clock which is phase coherent with said downstream clock, said upstream clock

9   having a frequency which is M/N times the frequency of said downstream clock,

10   where M and N are integers; and

11   third means for using said upstream clock to transmit upstream data to said

12   headend over said transmission media.

1   8. The apparatus of claim 7 wherein said third means includes means for

2   transmitting data upstream using synchronous code division multiplexing.

1   9. The apparatus of claim 7 wherein said third means includes means for

2   transmitting data upstream using time-division multiple access multiplexing.

1   10. The apparatus of claim 7 wherein said third means includes means for

2   transmitting data upstream using DMT multiple access multiplexing.

1   11. The apparatus of claim 7 wherein said third means includes means for

2   transmitting symbol data upstream using synchronous code division multiplexing by

3   mapping minislots assigned to said modem to one or more symbols and one or more

4   spreading codes.

1   12. The apparatus of claim 7 wherein said third means includes means for

2   transmitting symbol data upstream using DMT multiplexing by mapping minislots

3   assigned to said modem to one or more symbols and one or more frequencies.

1   13. A modem for use as a remote node in a bidirectional communication system

2   having a headend and a plurality of remote node coupled to said headend by a transmission

media, comprising:

first means for recovering a downstream clock from data transmitted by said headend over said transmission media and for using said recovered downstream clock to recover downstream data;

a clock for generating an upstream clock signal; and

third means for using said upstream clock signal to transmit upstream data to said headend over said transmission media.

14. The apparatus of claim 13 wherein said third means includes means for transmitting symbol data upstream using synchronous code division multiple access multiplexing by mapping minislots assigned to said modem to one or more symbols and one or more spreading codes.

15. The apparatus of claim 13 wherein said third means includes means for transmitting symbol data upstream using DMT multiplexing by mapping minislots assigned to said modem to one or more symbols and one or more frequencies.

16. The apparatus of claim 14 further comprising means for selectably altering the mapping.

17. The apparatus of claim 15 further comprising means for selectably altering the mapping.

18. A modem for use as a remote node in a bidirectional communication system having a headend and a plurality of remote node coupled to said headend by a transmission media, comprising:

first means for recovering a downstream clock from data transmitted by said headend over said transmission media and for using said recovered downstream clock to recover downstream data;

a clock for generating an upstream clock signal; and

third means for using said upstream clock signal to transmit upstream data to

9   said headend over said transmission media, and

10   wherein upstream data transmission is on the basis of assigned minislots counted

11   by a minislot counter in the headend, said minislot counter having a rollover value

12   that defines a superframe boundary, and further comprising ranging means for

13   carrying out the communications of a ranging algorithm to determine an offset value

14   for a symbol counter which also has a rollover value which defines a superframe of

15   symbols which exactly corresponds in duration with said superframe of minislots,

16   said symbol counter being implemented by said third means, said offset being of a

17   value which will cause transmission of symbol data upstream with timing such that

18   the superframe boundaries of a superframe of symbols transmitted upstream arrive

19   at said headend aligned in time with said superframe boundaries of said minislots..

1   19. The apparatus of claim 18 wherein said headend sends sync messages and UCD

2   messages downstream, each said sync message carrying a timestamp sample from a

3   timestamp counter in said headend and each said UCD message containing a timestamp at

4   the time of a kiloframe or superframe boundary occurring at said headend, and further

5   comprising means in said modem for calculating an initial offset value from a sync

6   message and a UCD message and for using said offset as an initial offset value or starting

7   point for said ranging means.

1   20. A system for bidirectional communication of digital data between a CU modem

2   and a plurality of RU modems, comprising:

3   a shared transmission media coupling said CU and RU modems; and

4   a CU modem comprising:

5   a master clock for generating a master clock signal;

6   first means for generating downstream clock signals;

7   second means coupled to said shared transmission media for receiving said

8   downstream clock signal and for using it to transmit downstream data over said

9   shared transmission media; and

10   third means coupled to said shared transmission media and for receiving

11   upstream data transmitted over said shared transmission media and recovering an

12   upstream clock and carrier therefrom and using said recovered upstream clock and

13   carrier signals to demodulate and demultiplex SCDMA multiplexed upstream symbols

14   having their spectrums spread with a plurality of spreading codes, said symbols and

15   spreading codes being mapped to minislots assigned by said CU modem to said RU

16   modem(s); and

17 an RU modem comprising

18   fourth means coupled to said shared transmission medium, for recovering a

19   downstream clock and downstream carrier from data transmitted by said CU modem

20   over said shared transmission media and for using said recovered downstream clock

21   and carrier to recover downstream data including said minislot assignments

22   transmitted from said CU modem;

23   a timebase for generating an upstream clock and upstream carrier;

24   fifth means coupled to said shared transmission media and to said timebase and to

25   said fourth means for mapping said minslot assignment to one or more symbols and

26   one or more spreading codes or DMT frequencies for use in transmitting symbols

27   upstream to said CU modem, and for using said upstream clock upstream carrier and

28   said symbols and spreading codes or DMT frequencies mapped to said minislot

29   assignment to transmit upstream data to said CU modem over said shared

30   transmission media.

1   21. A system for bidirectional communication of digital data between a CU modem

2   and a plurality of RU modems, comprising:

3   a shared transmission media coupling said CU and RU modems; and

4   a CU modem comprising:

5   a master clock for generating a master clock signal;

6   first means for generating upstream and downstream clock signals which are

7   phase coherent with said master clock signal, said upstream clock signal having a

8   frequency which is M/N times the frequency of said downstream clock signal, where

9   M and N are integers;

10   second means coupled to said shared transmission media for receiving said

11   downstream clock signal and for using it to transmit downstream data over said

12   shared transmission media; and

13   third means coupled to said shared transmission media and coupled to receive said

14   upstream clock signal and using it to receive upstream data transmitted over said

15   shared transmission media; and

16 an RU modem comprising

17   fourth means coupled to said shared transmission medium, for recovering a

18   downstream clock from data transmitted by said CU modem over said shared

19   transmission media and for using said recovered downstream clock to recover

20   downstream data;

21   fifth means for using said recovered downstream clock to generate an upstream

22   clock which is phase coherent with said downstream clock, said upstream clock

23   having a frequency which is M/N times the frequency of said downstream clock,

24   where M and N are integers; and

25   sixth means coupled to said shared transmission media for using said upstream

26   clock to transmit upstream data to said CU modem over said shared transmission

27   media.

1   22. A system for bidirectional communication of digital data between a CU modem

2 and a plurality of RU modems, comprising:

3   a shared transmission media coupling said CU and RU modems; and

4 a CU modem comprising:

5   a master clock for generating a master clock signal;

6   first means for generating upstream and downstream clock and carrier signals

7   which are phase coherent with said master clock signal, said upstream clock signal

8   having a frequency which is M/N times the frequency of said downstream clock

9   signal, where M and N are integers;

10   second means coupled to said shared transmission media for receiving said

11   downstream clock signal and said downstream carrier and for using them to transmit

12   downstream data over said shared transmission media; and

13   third means coupled to receive upstream signals transmitted over said shared

14   transmission media and coupled to receive said upstream clock signal and said

15   upstream carrier signal and using them to demodulate and demultiplex SCDMA

16   multiplexed upstream symbols in said upstream signals, said symbols having their

17   spectrums spread with a plurality of spreading codes, said symbols and spreading

18   codes being mapped to minislots assigned by said CU modem to said RU modem(s) for

19   upstream transmissions; and

20 an RU modem comprising

21   fourth means coupled to said shared transmission medium, for recovering a

22 downstream clock from data transmitted by said CU modem over said shared

23 transmission media and for using said recovered downstream clock to generate a

24 downstream carrier which is phase coherent with said downstream carrier signal

25 used by said second means to transmit said downstream data and using said

26 downstream clock and carrier signals to demodulate and recover downstream data

27 including said minislot assignment for upstream transmission;

28   fifth means for using said recovered downstream clock to generate an upstream

29 clock and an upstream carrier which are both phase coherent with said recovered

30 downstream clock, said upstream clock having a frequency which is M/N times the

31 frequency of said downstream clock, where M and N are integers; and

32   sixth means coupled to said shared transmission media for using said upstream

33 clock and upstream carrier signals to transmit upstream symbol data to said CU

34 modem over said shared transmission media by mapping said minslot assignment

35 received from said CU modem to one or more symbols and one or more spreading

36 codes or DMT frequencies for use in transmitting symbols upstream to said CU

37 modem, and for using said upstream clock upstream carrier and said symbols and

38 spreading codes or DMT frequencies mapped to said minislot assignment to transmit

39 upstream data to said CU modem over said shared transmission media.

1   23. The apparatus of claim 22 wherein said CU modem includes a minislot counter

2 which rolls over at a programmable count value which defines a superframe boundary,

3 and further comprises a timestamp counter, a timestamp sampler and a sync message

4 generator means for generating sync messages that contain samples taken by said

5 timestamp sampler of said timestamp counter from time to time and for generating UCD

6   messages which contain samples taken by said timestamp sampler of said timestamp

7   counter at superframe boundaries, and wherein said second means transmits said sync

8   messages and UCD messages downstream to said RU modem, and wherein said RU modem

9   includes a symbol counter coupled to or part of said sixth means which counts symbols in

1 0   a superframe of symbols that exactly corresponds in duration to said superframe of

1 1   minslots and which rolls over at a count corresponding to a boundary of a superframe of

1 2   symbols, and wherein fourth means includes offset calculation means for using said sync

1 3   messages and UCD messages to calculate an offset to load into said symbol counter such

1 4   that the superframe boundaries of a superframe of said symbols transmitted upstream

1 5   by said sixth means will be approximately superimposed in time at said CU modem with

1 6   the superframe boundaries of a superframe of minislots mapped to said superframe of

1 7   symbols.

1   24. The apparatus of claim 23 wherein said sixth means further comprises ranging

2   means for using said offset calculated by said offset calculation means as a starting point

3   to carry out a trial and error ranging process to determine an exact offset for said

4   symbol counter which will cause said superframe boundaries of a superframe of

5   upstream symbols to be exactly superimposed in time at said CU modem with the

6   superframe boundaries of a superframe of minislots mapped to said superframe of

7   symbols.

1   25. The apparatus of claim 22 wherein said CU modem includes a minislot counter

2   which rolls over at a count value which defines a superframe boundary, and wherein said

3   RU modem includes a symbol counter coupled to or part of said sixth means which counts

4   symbols in a superframe of symbols that exactly corresponds in duration to said

5   superframe of minslots and which rolls over at a count corresponding to a boundary of a

6   superframe of symbols, and wherein said sixth means further comprises ranging means

7   for determining an exact offset for said symbol counter which will cause said

8   superframe boundaries of a superframe of upstream symbols to be exactly superimposed

9   in time at said CU modem with the superframe boundaries of a superframe of minislots

1 0   mapped to said superframe of symbols.

1   26. The apparatus of claim 24 wherein downstream data arrives at said second

2   means in the form of packets with headers and wherein said second means further breaks

3   down said packets and headers into FEC frames having overhead bits and ECC error

4   detection and correction bits therein, and wherein said second means includes means for

5   inserting said sync messages and said UCD messages in the stream of downstream data so

6   as to have low jitter by monitoring the point of insertion of every sync or UCD message

7   into every packet based upon the length of the data and header portions of the packet and

8   the length of said sync or UCD message and changing the point of insertion whenever said

9   sync message or UCD message would not fit completely within the data portion of a packet

10   and would straddle a header portion, and by always inserting the sync message or UCD

11   message at the same point in every FEC frame such that whatever straddles of overhead

12   or ECC bits exist are always the same.

1   27. The apparatus of claim 22 further comprising a clock slip detector means

2   coupled to receive said recovered downstream clock and said upstream clock and for

3   counting and storing the count of the clock cycles of said upstream clock over each

4   predetermined interval of said recovered downstream clock and generating an interrupt

5   signal at the end of every interval.

1   28. The apparatus of claim 27 further comprising means for receiving said

2   interrupt signal and for retrieving the count of upstream clock cycles in response

3   thereto and comparing said count to a predetermined expected number, and if there is a

4   mismatch of more than a predetermined number of clock cycles, for causing said sixth

5   means to cease transmitting.

1   29. A process for transmitting data in both directions in a bidirectional digital data

2   communication system, comprising:

3   generating a master clock signal in a headend modem, and generating a

4   downstream clock and carrier signal from said master clock signal both of which are

5   phase coherent therewith, and generating an upstream clock and carrier signals in

6   said headend modem from said master clock signal both of which are phase coherent

7   therewith, said upstream clock signal having a frequency which is M/N times the

8   frequency of said downstream clock, where M and N are integers;

9   transmitting data downstream to a remote modem using said downstream clock

10   and carrier signals;

11   in said remote modem, recovering at least said downstream clock signal and using

12   it to recover downstream data, and using said recovered downstream clock signal to

13   generate an upstream clock signal and an upstream carrier signal both of which are

14   phase coherent with the recovered downstream clock signal, said upstream clock

15   signal having a frequency which is M/N times the frequency of said recovered

16   downstream clock signal;

17   using said upstream clock and carrier signals to transmit symbol data upstream

18   to a headend modem;

19   using said upstream clock and carrier signals generated in said head end modem to

20   recover upstream data transmitted from said remote node.

1   30. A process for mapping upstream symbols and spreading codes in an SCDMA

2   system to upstream assigned minislots comprising:

3   organizing data to be transmitted into frames comprised of subframes each of

4   which contains chips generated from symbols in an information vector, with one

5   information vector mapped to each subframe, and a programmable number of frames

6   mapped to every minislot;

7   counting minislots with a minislot counter that rolls over at some number which

8   defines a superframe of minislots;

9   setting a rollover count of a symbol counter to establish a superframe of symbols

10   such if said minislot counter and said symbol counter simultaneously started

11   counting from zero, both would roll over simultaneously;

12   mapping symbols and spreading codes to minislots by starting on a first code and

13   assigning numbers to symbols to each frame in accordance with how many subframes

14   there are in said frame and continuing this process with subsequent frames along a

15   time axis until a programmable value of L is reached where L is an integer, then

repeating the process starting with another code along a code axis and starting with

17   another frame until L is reached again and repeating this process until the number of

18   symbols in a superframe of symbols have been mapped to specific frames and

19   minislots and specific codes.

1   31. A process of transmitting SCDMA data in an upstream organized as numbered

2   minislots, comprising:

3   receiving a minislot assignment naming specific numbered minislots on which

4   transmission is authorized;

5   mapping the specific minislot numbers in said assignment to specific symbols

6   and spreading codes and frame and subframes that map to those minislots;

7   constructing one information vector for every subframe mapped to the minislot

8   assignment by placing the numbered symbols that map to the numbered minislots in

9   the assignment in the elements of the information vectors corresponding to the

10   numbered code each numbered symbol maps to;

11   spreading the spectrum of each information vector by matrix multiplication of

12   the information vector times a code matrix having a plurality of codes therein which

13   corresponds to the number of elements in the information vector to generate one

14   result vector for every subframe that maps to the assigned minislots; and

15   transmitting RF signals derived from the result vectors.